VLSI-SoC 2022 : Preliminary Program

Monday, October 3

Time	Session	Title	Authors
8:45		***Keynote: Designing Phase-Locked Loops in Modern CMOS Technologies ,*** Prof. Salvatore Levantino, Politecnico di Milano	
9:40 -- 11:20	M1A	***Systems on Chip***	
	M1A	*Embedded TCP/IP Controller for a RISC-V SoC*	Chun-Jen Tsai and Yi-De Lee
	M1A	*A Hardware-based HEFT Scheduler Implementation for Dynamic Workloads on Heterogeneous SoCs*	Alexander Fusco, Sahil Hassan, Joshua Mack and Ali Akoglu
	M1A	*RISC-V Processor Trace Encoder with Multiple Instructions Retirement Support*	Halil Kükner, Gökhan Kaplayan, Ahmet Efe and Mehmet Ali Gülden
	M1A	*RIBiT: Reduced Intra-flit Bit Transitions for Bufferless NoC*	Akshay Sarman, Alwin Shaju, Rose George Kunthara, Neethu K, Rekha K. James and John Jose
	M1B	***Design Automation - 1***	
	M1B	*Guiding FPGA Detailed Placement Via Reinforcement Learning*	Pooria Esmaeili, Timothy Martin, Shawki Areibi and Gary Grewal
	M1B	*Generation of Formal CPU Profiles for Embedded Systems*	Stian Sorensen, Christian Bartsch, Dominik Stoffel and Wolfgang Kunz
	M1B	*Simulation-Based Maximum Coverage Hazards Detection and Elimination Analysis, Supporting Combinational Logic Loops*	Nikolaos Chatzivangelis, Dimitris Valiantzas, Christos Sotiriou and Iordanis Lilitsis
	M1B	*Investigation on Performance, Power, Area Trade-Offs using Deterministic and Monte-Carlo Process Variation Aware Synthesis Flows*	Nikolaos Blias, Iordanis Lilitsis, Stavros Simoglou, Christos Sotiriou and Evangelos Bakas
		Break	
11:40 -- 13:20	SS1	***Special Session on Computation-in-Memory: Opportunities and challenges***	
	SS1	*FeFET versus DRAM based PIM Architectures: A Comparative Study*	Chirag Sudarshan, Taha Soliman, Thomas Kämpfe, Christian Weis and Norbert Wehn
	SS1	*Cross-layer FeFET Reliability Modeling for Robust Hyperdimensional Computing*	Shubham Kumar, Swetaki Chatterjee, Simon Thomann, Paul R. Genssler, Yogesh Singh Chauhan and Hussam Amrouch
	SS1	*System Design for Computation-in-Memory: From Primitive to Complex Functions*	Mahdi Zahedi, Taha Shahroodi, Abhairaj Singh, Geert Custers, Stephan Wong and Said Hamdioui
	SS2	***Special Session on Front-end circuits and subsystems for 5G applications***	
	SS2	*A Wideband High-Gain Power Amplifier Operating in the D Band*	Vasileios Manouras and Ioannis Papananos
	SS2	*Frequency Synthesizers for 5G Applications*	Salvatore Levantino
	SS2	*30 GHz Front-End with Adaptively Biased PA and Current Steering LNA for Phased Array Systems*	Panagiotis Gkoutis, Georgios Konidas and Grigorios Kalivas
		Poster 1 *	
		Lunch	
14:45 -- 16:25	M2A	***Digital Design***	
	M2A	*An Energy-Efficient Three-Independent-Gate FET Cell Library for Low-Power Edge Computing*	Michael Keyser, Roman Gauchi and Pierre-Emmanuel Gaillardon
	M2A	*A Low-Overhead Method for the Accurate Estimation of the Maximum Operating Clock Frequency*	Brent Bohnenstiehl, Aaron Stillmaker, Timothy Andreas and Bevan Baas
	M2A	*Exploring Approximate Comparator Circuits on Power Efficient Design of Decision Trees*	Pedro Silva, Mateus Grellert and Cristina Meinhardt
	M2A	*Hardware Accelerators for Processing Clusters in Binary Vectors*	Iouliia Skliarova and Valery Sklyarov
	M2B	***Design Automation - 2***	
	M2B	*Stitch-avoiding Detailed Routing for Multiple E-Beam Lithography*	Kritanta Saha, Pritha Banerjee and Susmita Sur-Kolay
	M2B	*SPTA: A Scalable Parallel ILP-Based Track Assignment Algorithm with Two-stage Partition*	Yidan Jing, Liliang Yang, Zhen Zhuang, Genggeng Liu, Xing Huang, Wen-Hao Liu and Ting-Chi Wang
	M2B	*FPGA-Based Stochastic Local Search Satisfiability Solvers Exploiting High Bandwidth Memory*	Christopher Chuvalas and Ranga Vemuri
	M2B	*LA-SVR: A High-Performance Layer Assignment Algorithm with Slew Violations Reduction*	Lieqiu Jiang, Zepeng Li, Chenpeng Bao, Genggeng Liu, Xing Huang, Wen-Hao Liu and Ting-Chi Wang
		Break	
	M3A	***Analog Design***	
	M3A	*Machine Learning based Power Converter Large Signal Simulation for Energy Harvesting Applications*	George Vergos, Vasiliki Gogolou, Christina Panagiotopoulou, Anastasios Avgoustidis, Thomas Noulis, Kostas Siozios and Stylianos Siskos
	M3A	*A Circuit-Level SPICE Modeling Strategy for the Simulation of Behavioral Variability in ReRAM*	Jose Cayo, Ioannis Vourkas and Antonio Rubio

Time	Session	Paper	Authors
16:50 -- 18:30		*A novel wide frequency range 65nm CMOS VCO*	Dimitrios Samaras, Andreas Tsimpos and Alkis Hatzopoulos
		A self-referenced on-chip jitter BIST with sub-picosecond resolution in 28 nm FD-SOI technology	Manasa Madhvaraj, Salvador Mir and Manuel J. Barragan
	M3B	***Circuits for Communications***	
		Architecture and 28 nm CMOS Design of a 1886 MBin/sec Context-Adaptive Binary Arithmetic Coder (CABAC) Encoder	Renjie Chen, Aaron Stillmaker and Bevan Baas
		High-Speed SC Decoder for Polar Codes achieving 1.7 Tb/s in 28 nm CMOS	Lukasz Lopacinski, Alireza Hasani, Goran Panic, Nebojsa Maletic, Jesus Gutiérrez, Milos Krstic and Eckhard Grass
		A FPGA implementation of the VESA Display Stream Compression decoder	Nikolaos Kefalas and George Theodoridis
		High-Level Synthesis design approach for Number-Theoretic Multiplier	Islam Aleaxnder El-Kady, Apostolos Fournaris and Vassilis Paliouras
		*** Papers in session Poster 1***	
		Gradient Backpropagation based Feature Attribution to Enable Explainable-AI on the Edge	Ashwin Bhat, Adou Sangbone Assoa and Arijit Raychowdhury
		ENDURA : Enhancing Durability of Multi Level Cell STT-RAM based Non Volatile Memory Last Level Caches	Yogesh Kumar, S Sivakumar and John Jose
		Flexible Security and Privacy, System Architecture for IoT, in Healthcare	Kyriaki Tsantikidou and Nicolas Sklavos
		Enabling Automotive Electrification on Heterogeneous Automotive Microcontroller using Virtual System Modelling	Rupali Hongekar, Ankita Gupta, Jayakrishna Guddeti and Meghashyam Ashwathnarayan
		A Comparison of SAT-based and SMT-based Frameworks for X-value Combinational Equivalence Checking	Raiyyan Malik, Shubham Baunthiyal, Puneet Kumar, Srinath J and Sneh Saurabh
		Linear and Periodic State Integrated Circuits Noise Simulation Benchmarking	Anastasios Michailidis, Thomas Noulis and Kostas Siozios
		Practical Day-Ahead Power Prediction of Solar Energy-Harvesting for IoT Systems	Konstantinos Falis, Andreas Tsiougkos and Vasilis F. Pavlidis
		Unlocking High Resolution Arithmetic Operations within Memristive Crossbars for Error Tolerant Applications	Kamalika Datta, Saman Froehlich, Dev Narayan Yadav, Saeideh Shirinzadeh, Indranil Sengupta and Rolf Drechsler
		A Power Reduction Technique Based on Linear Transformations for Cryptographic Block Ciphers	Elif Bilge Kavun
		Run Time Power and Accuracy Management with Approximate Circuits	Nahla El-Araby, David Frismuth, Nilson Neves Filho and Axel Jantsch
		Efficient Dynamic Logic Magnitude Comparators	Constantinos Efstathiou, Laura Agalioti and Yiorgos Tsiatouhas
		Power Analysis Attack on Locking SIB based IJTAG Achitecture	Gaurav Kumar, Anjum Riaz, Yamuna Prasad and Satyadev Ahlawat
		Hardware Trojan Mitigation for Securing On-chip Networks from Dead Flit Attacks	Gaurav Kumar, Anjum Riaz, Yamuna Prasad and Satyadev Ahlawat

Tuesday, October 4

Time	Session	Paper	Authors
8:45	***Keynote: Preserving Design Hierarchy Information for Polynomial Formal Verification ,*** Prof. Rolf Drechsler, University of Bremen		
9:40 -- 11:20	T1A	***Fault tolerance and testing***	
		Combining Fault Tolerance Techniques and COTS SoC Accelerators for Payload Processing in Space	Vasileios Leon, Elissaios Alexios Papatheofanous, George Lentaris, Charalampos Bezaitis, Nikolaos Mastorakis, Georgios Bampilis, Dionysios Reisis and Dimitrios Soudris
		Fast and accurate Model-Driven FPGA-based System-Level Fault Emulation	Endri Kaja, Nicolas Gerlin, Monideep Bora, Gabriel Rutsch, Keerthikumara Devarajegowda, Dominik Stoffel, Wolfgang Kunz and Wolfgang Ecker
		A Signal-Integrity Aware ATPG Flow to Generate High-Quality Patterns for Testing System-on-Chip Designs	Anu Asokan
		State feedback control of interval-valued fuzzy descriptor system subject to random occurred actuator failures	Mourad Kchaou and Badr Alshammari
		Modelling	
		A Multi-stage Hybrid Approach for Mapping Applications on Heterogeneous Multi-core Platforms	Andreas Emeretlis, George Theodoridis, Panayiotis Alefragis and Nikolaos Voros

	T1B	*MemCork: Exploration of Hybrid Memory Architectures for Intermittent Computing at the Edge*	Theo Soriano, David Novo, Guillaume Prenat, Gregory Di Pendina and Pascal Benoit
		NISTT: A Non-Intrusive SystemC-TLM 2.0 Tracing Tool	Nils Bosbach, Lukas Jünger, Jan Moritz Joseph and Rainer Leupers
		Exploiting clustering and decision-tree algorithms to mine LTL assertions containing non-boolean expressions	Samuele Germiniani and Graziano Pravadelli
	Break		
11:40 -- 13:20	SS3	***Special Session on Variability in ReRAM devices: mitigation and opportunities for exploitation***	
		End-to-end modelling of variability-aware neural networks based on resistive-switching memory arrays	Artem Glukhov, Nicola Lepri, Valerio Milo, Andrea Baroni, Cristian Zambelli, Piero Olivo, Eduardo Pérez, Christian Wenger and Daniele Ielmini
		Reliability-Aware Ratioed Logic Operations for Energy-Efficient Computational ReRAM	Carlos Fernandez and Ioannis Vourkas
		Dealing with Non-Idealities in Memristor Based Computation-In-Memory Designs	Anteneh Gebregiorgis, Abhairaj Singh, Sumit Diware, Rajendra Bishnoi and Said Hamdioui
		Substrate Effect on Low-frequency Noise of synaptic RRAM devices	Nikolaos Vasileiadis, Alexandros Mavropoulis, Panagiotis Loukas, Pascal Normand, Georgios Ch. Sirakoulis and Panagiotis Dimitrakis
	SS4	***Special Session on Computing Circuits and SoCs for Space Applications***	
		SoC FPGA Acceleration for Semantic Segmentation of Clouds in Satellite Images	Elissaios Alexios Papatheofanous, Philippos Tziolos, Vasileios Kalekis, Tzouma Amrou, Georgios Konstantoulakis, Georgios Venitourakis and Dionysios Reisis
		Towards Employing FPGA and ASIP Acceleration to Enable Onboard AI/ML in Space Applications	Vasileios Leon, George Lentaris, Dimitrios Soudris, Simon Vellas and Mathieu Bernou
		A low-power, radiation-hardened Single Event Effect rate detection System on a Chip for Real Time Monitoring of Single Event Effects on Low Earth Orbit satellites	Georgios Kottaras, Theodoros Sarris, Athanasios Psomoulis, Ilias Ioakeimidis, Angelos Papathanasiou, Dave Pitchford and Ingmar Sandberg
		High-Performance Hardware Accelerators for Next Generation On-Board Data Processing	Antonios Paschalis and Nektarios Kranitis
	Poster 2: PhD and Students Forum **		
	Lunch		
	Social program: Visit to Olympia		
	Social program: Gala Diner		
		*****Papers in Session Poster 2: PhD and Student Forum***	
		Assessing IMD of a Direct-to-RF Platform	Jonathan Merk, Changhai Lin and Matthias Kamuf
		Investigation of Hybrid Soft Error Mitigation Techniques for Applications running on Resource-constrained devices	Jonas Gava, Ricardo Reis and Luciano Ost
		Analysis of an Inverter Logic Cell based on 3D Vertical NanoWire Junction-Less Transistors	Lucas Réveil, Chhandak Mukherjee, Cristell Maneux, Marina Deng, François Marc, Abhishek Kumar, Aurélie Lecestre, Guilhem Larrieu, Arnaud Poittevin, Ian O'Connor, Oskar Baumgartner and David Pirker
		Systematic Embedded Development and Implementation Techniques on Intel Myriad VPUs	Vasileios Leon, Kiamal Pekmestzi and Dimitrios Soudris
		Architectural Support for Functional Programming	Cecil Accetti and Peilin Liu
		Towards CIM-friendly and Energy-Efficient DNN Accelerator via Bit-level Sparsity	Foroozan Karimzadeh and Arijit Raychowdhury
		On the Design and Development of a ReRAM-based Computational Memory Prototype	Carlos Fernandez and Ioannis Vourkas
		A 18-27 GHz Programmable Gain Amplifier in 65-nm CMOS technology	Carolina del Río Bueno, Uxua Esteban Eraso, Santiago Celma Pueyo and Carlos Sánchez-Azqueta
		Speculative guardband: exploiting critical-delay variations across cached instructions	Johannes Warwick Farias, Diego V. C. Nascimento, Tiago Barros and Samuel Xavier-de-Sousa
		Routability-Driven Detailed Placement Using Reinforcement Learning	Sheiny Fabre Almeida, José Luís Güntzel, Laleh Behjat and Cristina Meinhardt
		Analog Compute in Memory and Breaking Digital Number Representations	Nathan Laubeuf
		A CMOS 4-bit Digitally Programmable Phase Shifter for the K-band	Uxua Esteban Eraso, Carlos Sánchez-Azqueta, Concepción Aldea and Santiago Celma
		Automated Framework for Fast Synthesis of Approximate Hardware Accelerators	Muhammad Awais and Marco Platzner

	Modeling frequency response of gm-boosted inductorless Common-Gate LNA	Jorge Marqués-García, Alberto Arcusa-Puente, Antonio D. Martínez-Pérez and Francisco Aznar
	Exploring Approximate Computing Approaches to Design Power-efficient Multipliers	Vinícius Zanandrea and Cristina Meinhardt
	Approximation Workflow for Energy-Efficient Comparators in Decision Tree Applications	Pedro Silva, Mateus Grellert and Cristina Meinhardt
	Design and characterisation of a Physically Unclonable Function on FPGA using second-order compensated measurement	Jorge Fernandez-Aragon, Guillermo Diez-Senorans, Miguel Garcia-Bosque and Santiago Celma

	Wednesday, October 5		
8:45	***Keynote:Challenges in Hardware Implementations of Fully Homomorphic Encryption Algorithms ,*** Prof. Çetin Kaya Koç, University of California, Santa Barbara		
9:40 -- 11:20	W1A	***Artificial Intelligence and Machine Learning - 1***	
	W1A	*P2M-DeTrack: Processing-in-Pixel-in-Memory for Real-Time and Energy-Efficient Multi-Object Detection and Tracking*	Gourav Datta, Souvik Kundu, Zihan Yin, Joe Mathai, Zeyu Liu, Zixu Wang, Mulin Tian, Shunlin Lu, Ravi T. Lakkireddy, Andrew Schmidt, Wael Abd-Almageed, Ajey P. Jacob, Akhilesh R. Jaiswal and Peter A. Beerel
	W1A	*Towards Energy Efficient DNN accelerator via Sparsified Gradual Knowledge Distillation*	Foroozan Karimzadeh and Arijit Raychowdhury
	W1A	*Energy-Efficient SNN Implementation Using RRAM-Based Computation In-Memory (CIM)*	Asmae El Arrassi, Anteneh Gebregiorgis, Anass El Haddadi and Said Hamdioui
	W1A	*High Level Synthesis Acceleration of Change Detection in Multi-Temporal High Resolution Sentinel-2 Satellite Images*	Konstantina Koliogeorgi, Dimitris Mylonakis, Sotirios Xydis and Dimitrios Soudris
	W1B	***Hardware for security***	
	W1B	*PA-PUF: A Novel Priority Arbiter PUF*	Simranjeet Singh, Srinivasu Bodapati, Sachin Patkar, Rainer Leupers, Anupam Chattopadhyay and Farhad Merchant
	W1B	*Design of a Tightly-Coupled RISC-V Physical Memory Protection Unit for Online Error Detection*	Nicolas Gerlin, Endri Kaja, Monideep Bora, Keerthikumara Devarajegowda, Dominik Stoffel, Wolfgang Kunz and Wolfgang Ecker
	W1B	*Towards Generic Power/EM Side-Channel Attacks: Memory Leakage on General-Purpose Computers*	Can Aknesil and Elena Dubrova
	W1B	*Logic Locking of Finite-State Machines Using Transition Obfuscation*	Shahzad Muzaffar and Ibrahim Elfadel
	Break		
11:40 -- 13:20	W2A	***Artificial Intelligence and Machine Learning - 2***	
	W2A	*ZaLoBI: Zero avoiding Load Balanced Inference accelerator*	Imlijungla Longchar, Palash Das and Hemangee K. Kapoor
	W2A	*Toward Large Scale All-Optical Spiking Neural Networks*	Milad Eslaminia and Sébastien Le Beux
	W2A	*FPGA-SoC deployment of complex deep neural network for magnitude and phase computations in denoising of speech signal*	Georgios Flamis, Stavros Kalapothas and Paris Kitsos
	W2A	*Confidential Inference in Decision Trees: FPGA Design and Implementation*	Rupesh Karn and Ibrahim Elfadel
	SS5	***Special Session on Key enabling technologies for the physical-layer of 6G communications***	
	SS5	*Secrecy spectral efficiency optimization in RIS-enabled MIMO Communication Systems*	Konstantinos D. Katsanos and George C. Alexadropoulos
	SS5	*Accurate real-time UAV flight-mode classification*	Nikolaos Georgiou and Panayiotis Kolios
	SS5	*Quantum computing-assisted Channel Estimation for Millimeter-Wave Massive MIMO Communications*	Evangelos Vlachos and Kostas Blekos
	Awards and farewell		
	Lunch		